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EXAMINER	
GUILL, RUSSELL L	

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2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/994,574	WHEELER ET AL.	
	Examiner	Art Unit	
	Russell L. Guill	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date [redacted]. 9 Pages
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 25 have been examined. Claims 1 – 25 have been rejected.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding claim 15, claim 15 recites, "the central database**s**". There is insufficient antecedent basis for the term. For the purpose of claim interpretation, the phrase, "the central database**s**" is interpreted as "the central database". Correction or amendment is required.

Claim Rejections – 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 1 - 6 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claims appear to produce an intangible result.

6. Claims 7 - 14 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claims appear to produce an intangible result.

7. Claims 15 - 17 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claims appear to produce an intangible result.

8. Claims 18 - 25 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claim 18 recites, "A machine-accessible medium, which when accessed results in a machine performing operations". For the purpose of claim interpretation, the phrase is interpreted as "A computer readable medium containing instructions which cause a computer to perform operations". Claims 19 – 25 are dependent upon claim 18, and thereby inherit all of the rejected limitations of claim 18.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over ExpressiveSystems (Internet Archive Wayback Machine, www.archive.org, search for www.expressivesystems.com, February 8, 2001) in view of Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference).

10.1. The art of ExpressiveSystems is directed to logic design systems ***(page 2)***.

10.2. The art of Yamagishi is directed to logic design systems ***(page 13.2.1, Abstract, and section 1 Introduction)***.

10.3. ExpressiveSystems appears to teach a logic design module operational to be used by one or more users in logic design tasks ***(page 1, first and second paragraphs)***.

10.4. ExpressiveSystems appears to teach signal parameters that are accessible to use by the users of the logic design module in the logic design tasks ***(page 8 and page 9)***.

10.5. ExpressiveSystems does not specifically teach ***a central database integrated with the logic design module*** and including signal parameters that are accessible to use by the users of the logic design module in the logic design tasks.

10.6. Yamagishi appears to teach a central database integrated with the logic design module ***(pages 13.2.2 and 13.2.3, section 2.2 Database FALNET)***.

10.7. ExpressiveSystems and Yamagishi are analogous art because they are both directed to the art of logic design systems.

10.8. The motivation to use the art of Yamagishi with the art of ExpressiveSystems would have been obvious given the statement in Yamagishi that the database allows much closer integration among tools than other commercially available frameworks ***(page 13.2.3, left-side of page, lines 1 – 3)***, and the expressed benefit in ExpressiveSystems of the software to save designers time and effort by simplifying the maintenance of the design ***(page 2, second paragraph)***.

11. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over ExpressiveSystems (Internet Archive Wayback Machine, www.archive.org, search for www.expressivesystems.com, February 8, 2001) and Yamagishi (Yamagishi, Kunihiko;

Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference).

11.1. Claim 2 is a dependent claim of claim 1, and thereby inherits all of the rejected limitations of claim 1.

11.2. ExpressiveSystems appears to teach that the central database includes modifications to the signal parameters ***(page 8 and page 9)***.

11.3. ExpressiveSystems appears to teach a logic design module that is structured and arranged to generate a logic design and to update the logic design automatically based on the modifications to the signal parameters in the central database ***(page 23 and page 24 and page 25)***.

11.3.1. Regarding ***(page 23 and page 24 and page 25)***; the recited pages demonstrate a modification of the signal database followed by generation of logic design code.

12. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over ExpressiveSystems (Internet Archive Wayback Machine, www.archive.org, search for www.expressivesystems.com, February 8, 2001) and Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference) in view of IEEEVerilog (IEEE Standard Hardware Description Language Based on the Verilog® Hardware Description Language, 1995, IEEE).

12.1. Claim 3 is a dependent claim of claim 2, and thereby inherits all of the rejected limitations of claim 2.

12.2. The art of ExpressiveSystems is directed to logic design systems ***(page 2)***.

12.3. The art of IEEEVerilog is directed to logic design ***(page iii, section Introduction)***.

12.4. ExpressiveSystems does not specifically teach that the logic design module is structured and arranged to indicate design discrepancies automatically in the logic design resulting from the modifications to the signal parameters in the central database.

12.5. Yamagishi appears to teach a central database integrated with the logic design module ***(pages 13.2.2 and 13.2.3, section 2.2 Database FALNET).***

12.6. IEEEVerilog appears to teach indicating design discrepancies automatically in the logic design resulting from the modifications to the signal parameters ***(page 59, lines 1 – 25)***.

12.6.1. Regarding ***(page 59, lines 1 – 25)***; it is obvious that updating a signal bit width incorrectly for terminal connections would result in too few or too many bits to connect all the instances, which would cause an error.

12.7. ExpressiveSystems and IEEEVerilog are analogous art because they both include the problem of logic design.

12.8. The motivation to use the art of IEEEVerilog with the art of ExpressiveSystems would have been obvious since:

12.8.1. ExpressiveSystems generates Verilog computer code ***(page 24 and page 25)***, and IEEEVerilog validates and executes Verilog computer code, and

12.8.2. given the expressed benefit in ExpressiveSystems that the software saves designers time and effort by simplifying the maintenance of the design ***(page 2, second paragraph)***, and

12.8.3. indicating design discrepancies earlier in the design before generating Verilog computer code would save time and effort.

12.9. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of ExpressiveSystems with the art of IEEEVerilog to produce the claimed invention.

13. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over ExpressiveSystems (Internet Archive Wayback Machine, www.archive.org, search for www.expressivesystems.com, February 8, 2001) and Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference) and IEEEVerilog (IEEE Standard Hardware Description Language Based on the Verilog® Hardware Description Language, 1995, IEEE).

13.1. Claim 4 is a dependent claim of claim 3, and thereby inherits all of the rejected limitations of claim 3.

13.2. ExpressiveSystems appears to teach indicating a bit width ***(page 24, screen displayed at top of page, the bit width is embedded in the line)***.

13.3. ExpressiveSystems does not specifically teach indicating a bit width ***error***.

13.4. IEEEVerilog appears to teach indicating a bit width error ***(page 59, lines 1 – 25)***.

13.4.1. Regarding ***(page 59, lines 1 – 25)***; it is obvious that updating a signal bit width incorrectly for terminal connections would result in too few or too many bits to connect all the instances, which would cause an error.

13.5. Therefore, as discussed above, it would have been obvious to use the art of IEEEVerilog with the art of ExpressiveSystems to obtain the invention of claim 4.

14. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over ExpressiveSystems (Internet Archive Wayback Machine, www.archive.org, search for www.expressivesystems.com, February 8, 2001) and Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference).

14.1. Claim 5 is a dependent claim of claim 1, and thereby inherits all of the rejected limitations of claim 1.

14.2. ExpressiveSystems appears to teach that the signal parameters include a signal bit width and a value for the signal bit width ***(page 23, on the Net Editor screen, in the field labeled New Signal(s), a signal is named dBus with a width of 32. This may be confirmed by examining the code generated on page 25)***.

15. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over ExpressiveSystems (Internet Archive Wayback Machine, www.archive.org, search for www.expressivesystems.com, February 8, 2001) and Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference).

15.1. Claim 6 is a dependent claim of claim 1, and thereby inherits all of the rejected limitations of claim 1.

15.2. ExpressiveSystems appears to teach that the signal parameters include a signal bit position and a value for the signal bit position ***(page 14, section labeled 'Flexible signal handling')***.

16. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over ExpressiveSystems (Internet Archive Wayback Machine, www.archive.org, search for

www.expressivesystems.com, February 8, 2001) in view of Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference).

16.1. The art of ExpressiveSystems is directed to logic design systems ***(page 2)***.

16.2. The art of Yamagishi is directed to logic design systems ***(page 13.2.1, Abstract, and section 1 Introduction)***.

16.3. ExpressiveSystems appears to teach defining a signal parameter with a value ***(page 8 and page 9)***.

16.4. ExpressiveSystems appears to teach maintaining the defined signal value ***(page 8 and page 9)***.

16.5. ExpressiveSystems appears to teach using the defined signal parameter in computer code for a logic design ***(page 23 and page 24 and page 25 - page 23, on the Net Editor screen, in the field labeled New Signal(s), a signal is named dBus with a width of 32)***.

16.5.1. Regarding ***(page 23 and page 24 and page 25 - page 23, on the Net Editor screen, in the field labeled New Signal(s), a signal is named dBus with a width of 32)***; the pages recited demonstrate defining a signal parameter followed by generation of computer code for logic design.

16.6. ExpressiveSystems does not specifically teach maintaining the defined signal value ***in a central database***.

16.7. ExpressiveSystems does not specifically teach using the defined signal parameter ***that is maintained in the central database*** in computer code for a logic design.

16.8. Yamagishi appears to teach a central database integrated with the logic design module ***(pages 13.2.2 and 13.2.3, section 2.2 Database FALNET)***.

16.9. ExpressiveSystems and Yamagishi are analogous art because they are both directed to the art of logic design systems.

16.10. The motivation to use the art of Yamagishi with the art of ExpressiveSystems would have been obvious given the statement in Yamagishi that the database allows much closer integration among tools than other commercially available frameworks ***(page 13.2.3, left-side of page, lines 1 – 3)***, and the expressed benefit in ExpressiveSystems of the software to save designers time and effort by simplifying the maintenance of the design ***(page 2, second paragraph)***.

16.11. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Yamagishi with the art of ExpresiveSystems to obtain the claimed invention.

17. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over ExpressiveSystems (Internet Archive Wayback Machine, www.archive.org, search for www.expressivesystems.com, February 8, 2001) and Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference).

17.1. Claim 8 is a dependent claim of claim 7, and thereby inherits all of the rejected limitations of claim 7.

17.2. ExpressiveSystems appears to teach updating the value of the defined signal parameter in the central database ***(page 8, view of screen)***.

17.3. ExpressiveSystems appears to teach automatically updating a logic design with the value of the updated signal parameter ***(page 23 and page 24 and page 25)***.

17.3.1. Regarding ***(page 23 and page 24 and page 25)***: the pages recited demonstrate defining a signal parameter of the signal database followed by updating of computer code for logic design. It is obvious that the computer code for logic design is generated using the stored value of the signal parameter, so that the computer code for logic design would be generated using an updated signal parameter.

18. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over ExpressiveSystems (Internet Archive Wayback Machine, www.archive.org, search for www.expressivesystems.com, February 8, 2001) and Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference) in view of IEEEVerilog (IEEE Standard Hardware Description Language Based on the Verilog® Hardware Description Language, 1995, IEEE).

18.1. Claim 9 is a dependent claim of claim 7, and thereby inherits all of the rejected limitations of claim 7.

18.2. The art of ExpressiveSystems is directed to logic design systems ***(page 2)***.

18.3. The art of IEEEVerilog is directed to logic design ***(page iii, section Introduction)***.

18.4. ExpressiveSystems does not specifically teach automatically indicating design discrepancies in the logic design that result from updating the value of the defined signal parameter.

18.5. IEEEVerilog appears to teach indicating design discrepancies automatically in the logic design resulting from the modifications to the signal parameters ***(page 59, lines 1 -- 25)***.

18.5.1. Regarding ***(page 59, lines 1 - 25)***; it is obvious that updating a signal bit width incorrectly for terminal connections would result in too few or too many bits to connect all the instances, which would cause an error.

18.6. ExpressiveSystems and IEEEVerilog are analogous art because they both are directed to the problem of logic design.

18.7. The motivation to use the art of IEEEVerilog with the art of ExpressiveSystems would have been obvious since:

18.7.1. ExpressiveSystems generates Verilog computer code ***(page 24 and page 25)***, and IEEEVerilog executes Verilog computer code, and

18.7.2. given the expressed benefit in ExpressiveSystems that the software saves designers time and effort by simplifying the maintenance of the design ***(page 2, second paragraph)***, and

18.7.3. indicating design discrepancies earlier in the design before generating Verilog computer code would save time and effort.

18.8. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of ExpressiveSystems with the art of IEEEVerilog to produce the claimed invention.

19. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over ExpressiveSystems (Internet Archive Wayback Machine, www.archive.org, search for

www.expressivesystems.com, February 8, 2001) and Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference) in view of IEEEVerilog (IEEE Standard Hardware Description Language Based on the Verilog® Hardware Description Language, 1995, IEEE).

19.1. Claim 10 is a dependent claim of claim 9, and thereby inherits all of the rejected limitations of claim 9.

19.2. ExpressiveSystems appears to teach graphically indicating a bit width ***(page 24, screen displayed at top of page, the bit width is embedded in the line)***.

19.3. ExpressiveSystems does not specifically teach indicating a bit width ***error***.

19.4. IEEEVerilog appears to teach indicating a bit width error ***(page 59, lines 1 – 25)***.

19.4.1. Regarding ***(page 59, lines 1 – 25)***; it is obvious that updating a signal bit width incorrectly for terminal connections would result in too few or too many bits to connect all the instances, which would cause an error.

19.5. Therefore, as discussed above, it would have been obvious to use the art of IEEEVerilog with the art of ExpressiveSystems to obtain the invention of claim 10.

20. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over ExpressiveSystems (Internet Archive Wayback Machine, www.archive.org, search for www.expressivesystems.com, February 8, 2001) and Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference).

20.1. Claim 11 is a dependent claim of claim 7, and thereby inherits all of the rejected limitations of claim 7.

20.2. ExpressiveSystems appears to teach that the signal parameter includes a signal bit width and the value includes a value for the signal bit width ***(page 23, on the Net Editor screen, in the field labeled New Signal(s), a signal is named dBus with a width of 32. This may be confirmed by examining the code generated on page 25)***.

21. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over ExpressiveSystems (Internet Archive Wayback Machine, www.archive.org, search for www.expressivesystems.com, February 8, 2001) and Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference).

21.1. Claim 12 is a dependent claim of claim 7, and thereby inherits all of the rejected limitations of claim 7.

21.2. ExpressiveSystems appears to teach that the signal parameter includes a signal bit position and the value includes a value for the signal bit position ***(page 14, section labeled 'Flexible signal handling', 'Multi-bit signals can be created with non-zero starting indexes', and page 8, on the signal display window, in the column labeled 'Signal Name', the signal named IO_DATA[15:0])***.

22. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over ExpressiveSystems (Internet Archive Wayback Machine, www.archive.org, search for www.expressivesystems.com, February 8, 2001) and Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference).

22.1. Claim 13 is a dependent claim of claim 7, and thereby inherits all of the rejected limitations of claim 7.

22.2. ExpressiveSystems appears to teach that the signal parameter includes a bit field and the value includes a value for the bit field ***(page 14, section labeled 'Flexible signal handling', 'Multi-bit signals can be created with non-zero starting indexes', and page 8, on the signal display window, in the column labeled 'Signal Name', the signal named IO_DATA[15:0])***.

23. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over ExpressiveSystems (Internet Archive Wayback Machine, www.archive.org, search for www.expressivesystems.com, February 8, 2001) and Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference).

23.1. Claim 14 is a dependent claim of claim 7, and thereby inherits all of the rejected limitations of claim 7.

23.2. Yamagishi appears to teach accessing the central database by one or more users ***(page 13.2.1, figure 1)***.

24. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over ExpressiveSystems (Internet Archive Wayback Machine, www.archive.org, search for www.expressivesystems.com, February 8, 2001) in view of Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference).

24.1. The art of ExpressiveSystems is directed to logic design systems ***(page 2)***.

24.2. The art of Yamagishi is directed to logic design systems ***(page 13.2.1, Abstract, and section 1 Introduction)***.

24.3. ExpressiveSystems appears to teach defining a signal parameter with a value ***(page 8 and page 9)***.

24.4. ExpressiveSystems appears to teach defining one or more signal parameters ***(page 8 and page 9)***.

24.5. ExpressiveSystems appears to teach a value for the signal parameters ***(page 8 and page 9)***.

24.6. ExpressiveSystems appears to teach a logic design module that uses the signal parameters ***(page 23 and page 24 and page 25 - page 23, on the Net Editor screen, in the field labeled New Signal(s), a signal is named dBus with a width of 32)***.

24.6.1. Regarding ***(page 23 and page 24 and page 25 - page 23, on the Net Editor screen, in the field labeled New Signal(s), a signal is named dBus with a width of 32)***; the pages recited demonstrate defining a signal parameter followed by generation of computer code for logic design.

24.7. ExpressiveSystems does not specifically ***a central database accessible by one or more users.***

24.8. ExpressiveSystems does not specifically teach one or more signal parameters defined ***in the central database***.

24.9. ExpressiveSystems does not specifically teach ***an interface between the central databases and*** a logic design module that uses the signal parameters in a logic design.

24.10. Yamagishi appears to teach a central database accessible by one or more users ***(page 13.2.1, figure 1, and pages 13.2.2 and 13.2.3, section 2.2 Database FALNET)***.

24.11. Yamagishi appears to teach logic design data stored in a central database ***(page 13.2.1, section 2 FALcyber)***.

24.12. Yamagishi appears to teach an interface between the central databases and a logic design module ***(pages 13.2.2 and 13.2.3, section 2.2 Database FALNET)***.

24.13. ExpressiveSystems and Yamagishi are analogous art because they are both directed to the art of logic design systems.

24.14. The motivation to use the art of Yamagishi with the art of ExpressiveSystems would have been obvious given the statement in Yamagishi that the database allows much closer integration among tools than other commercially available frameworks ***(page 13.2.3, left-side of page, lines 1 – 3)***, and the expressed benefit in ExpressiveSystems of the software to save designers time and effort by simplifying the maintenance of the design ***(page 2, second paragraph)***.

24.15. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Yamagishi with the art of ExpresiveSystems to obtain the claimed invention.

25. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over ExpressiveSystems (Internet Archive Wayback Machine, www.archive.org, search for www.expressivesystems.com, February 8, 2001) and Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference).

25.1. Claim 16 is a dependent claim of claim 15, and thereby inherits all of the rejected limitations of claim 15.

25.2. ExpressiveSystems appears to teach that the signal parameters include a signal bit width and the value includes a value for the signal bit width ***(page 23, on the Net Editor screen, in the field labeled New Signal(s), a signal is named dBus with a width of 32. This may be confirmed by examining the code generated on page 25)***.

26. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over ExpressiveSystems (Internet Archive Wayback Machine, www.archive.org, search for www.expressivesystems.com, February 8, 2001) and Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference).

26.1. Claim 17 is a dependent claim of claim 15, and thereby inherits all of the rejected limitations of claim 15.

26.2. ExpressiveSystems appears to teach that the signal parameters include a signal bit position and the value includes a value for the signal bit position ***(page 14, section labeled 'Flexible signal handling', 'Multi-bit signals can be created with non-zero starting indexes', and page 8, on the signal display window, in the column labeled 'Signal Name', the signal named IO_DATA[15:0])***.

27. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over ExpressiveSystems (Internet Archive Wayback Machine, www.archive.org, search for www.expressivesystems.com, February 8, 2001) in view of Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference).

27.1. The art of ExpressiveSystems is directed to logic design systems ***(page 2)***.

27.2. The art of Yamagishi is directed to logic design systems ***(page 13.2.1, Abstract, and section 1 Introduction)***.

27.3. ExpressiveSystems appears to teach defining a signal parameter with a value ***(page 8 and page 9)***.

27.4. ExpressiveSystems appears to teach maintaining the defined signal parameter ***(page 8 and page 9)***.

27.5. ExpressiveSystems appears to teach using the defined signal parameter in computer code for a logic design ***(page 23 and page 24 and page 25 - page 23, on the Net Editor screen, in the field labeled New Signal(s), a signal is named dBus with a width of 32)***.

27.5.1. Regarding ***(page 23 and page 24 and page 25 - page 23, on the Net Editor screen, in the field labeled New Signal(s), a signal is named dBus with a width of 32)***; the pages recited demonstrate defining a signal parameter of the signal database followed by generation of computer code for logic design.

27.6. ExpressiveSystems does not teach specifically using the defined signal parameter ***that is maintained in the central database*** in computer code for a logic design.

27.7. ExpressiveSystems does not teach specifically teach maintaining the defined signal parameter ***in a central database***.

27.8. Yamagishi appears to teach maintaining logic design data in a central database ***(page 13.2.1, section 2 FALcyber, and pages 13.2.2 and 13.2.3, section 2.2 Database FALNET)***.

27.9. ExpressiveSystems and Yamagishi are analogous art because they are both directed to the art of logic design systems.

27.10. The motivation to use the art of Yamagishi with the art of ExpressiveSystems would have been obvious given the statement in Yamagishi that the database allows much closer integration among tools than other commercially available frameworks ***(page 13.2.3, left-side of page, lines 1 – 3)***, and the expressed benefit in ExpressiveSystems of the software to save designers time and effort by simplifying the maintenance of the design ***(page 2, second paragraph)***.

27.11. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Yamagishi with the art of ExpresiveSystems to obtain the claimed invention.

28. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over ExpressiveSystems (Internet Archive Wayback Machine, www.archive.org, search for www.expressivesystems.com, February 8, 2001) and Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference).

28.1. Claim 19 is a dependent claim of claim 18, and thereby inherits all of the rejected limitations of claim 18.

28.2. ExpressiveSystems appears to teach updating the value of the defined signal parameter in the central database ***(page 8, view of screen)***.

28.3. ExpressiveSystems appears to teach automatically updating a logic design with the updated value of the defined signal parameter ***(page 23 and page 24 and page 25)***.

28.3.1. Regarding ***(page 23 and page 24 and page 25)***; the pages recited demonstrate updating a signal parameter of the signal database followed by updating of computer code for logic design. It is obvious that the signal parameter used to generate computer code for logic design uses the stored value of the signal parameter, so the updated value would be used to generate the logic design.

29. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over ExpressiveSystems (Internet Archive Wayback Machine, www.archive.org, search for www.expressivesystems.com, February 8, 2001) and Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference) in view of IEEEVerilog (IEEE Standard Hardware Description Language Based on the Verilog® Hardware Description Language, 1995, IEEE).

29.1. Claim 20 is a dependent claim of claim 19, and thereby inherits all of the rejected limitations of claim 19.

29.2. The art of ExpressiveSystems is directed to logic design ***(page 2)***.

29.3. The art of IEEEVerilog is directed to logic design ***(page iii, section Introduction)***.

29.4. ExpressiveSystems does not specifically teach automatically indicating design discrepancies occurring in the logic design that result from updating the value of the defined signal parameter.

29.5. IEEEVerilog appears to teach automatically indicating design discrepancies occurring in the logic design that result from updating the value of the defined signal parameter ***(page 59, lines 1 – 25)***.

29.5.1. Regarding ***(page 59, lines 1 – 25)***, it is obvious that updating a signal bit width incorrectly for terminal connections would result in too few or too many bits to connect all the instances, which would cause an error.

29.6. ExpressiveSystems and IEEEVerilog are analogous art because they are both directed to the art of logic design.

29.7. The motivation to use the art of IEEEVerilog with the art of ExpressiveSystems would have been obvious since:

29.7.1. ExpressiveSystems generates Verilog computer code ***(page 24 and page 25)***, and

29.7.2. given the expressed benefit in ExpressiveSystems that the software saves designers time and effort by simplifying the maintenance of the design ***(page 2, second paragraph)***.

29.7.3. Indicating design discrepancies earlier in the design before generating Verilog computer code would save time and effort.

30. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over ExpressiveSystems (Internet Archive Wayback Machine, www.archive.org, search for www.expressivesystems.com, February 8, 2001) and Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference) and IEEEVerilog (IEEE Standard Hardware Description Language Based on the Verilog® Hardware Description Language, 1995, IEEE).

30.1. Claim 21 is a dependent claim of claim 20, and thereby inherits all of the rejected limitations of claim 20.

30.2. ExpressiveSystems appears to teach graphically indicating a bit width ***(page 24, screen displayed at top of page)***.

30.3. ExpressiveSystems does not specifically teach graphically indicating a bit width ***error***.

30.4. IEEEVerilog appears to teach indicating a bit width error ***(page 59, lines 1 – 25)***.

30.4.1. Regarding ***(page 59, lines 1 – 25)***; it is obvious that updating a signal bit width incorrectly for terminal connections would result in too few or too many bits to connect all the instances, which would cause an error.

30.5. Therefore, as discussed above, it would have been obvious to use the art of IEEEVerilog with the art of ExpressiveSystems to obtain the invention of claim 21.

31. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over ExpressiveSystems (Internet Archive Wayback Machine, www.archive.org, search for www.expressivesystems.com, February 8, 2001) and Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference).

31.1. Claim 22 is a dependent claim of claim 18, and thereby inherits all of the rejected limitations of claim 18.

31.2. ExpressiveSystems appears to teach that the signal parameter includes a signal bit width and the value includes a value for the signal bit width ***(page 23, on the Net Editor screen, in the field labeled New Signal(s), a signal is named dBus with a width of 32. This may be confirmed by examining the code generated on page 25)***.

32. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over ExpressiveSystems (Internet Archive Wayback Machine, www.archive.org, search for www.expressivesystems.com, February 8, 2001) and Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference).

32.1. Claim 23 is a dependent claim of claim 18, and thereby inherits all of the rejected limitations of claim 18.

32.2. ExpressiveSystems appears to teach that the signal parameter includes a signal bit position and the value includes a value for the signal bit position ***(page 14, section labeled 'Flexible signal handling', 'Multi-bit signals can be created with non-zero starting indexes')***.

33. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over ExpressiveSystems (Internet Archive Wayback Machine, www.archive.org, search for www.expressivesystems.com, February 8, 2001) and Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference).

33.1. Claim 24 is a dependent claim of claim 18, and thereby inherits all of the rejected limitations of claim 18.

33.2. ExpressiveSystems appears to teach that the signal parameter includes a bit field and the value includes a value for the bit field ***(page 14, section labeled 'Flexible signal handling', 'Multi-bit signals can be created with non-zero starting indexes', and page 8, on the signal display window, in the column labeled 'Signal Name', the signal named IO_DATA[15:0])***.

34. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over ExpressiveSystems (Internet Archive Wayback Machine, www.archive.org, search for www.expressivesystems.com, February 8, 2001) and Yamagishi (Yamagishi, Kunihiko; Sekine, Masatoshi; A multi-representational design data capture system, 1993, IEEE 1993 Custom Integrated circuits conference).

34.1. Claim 25 is a dependent claim of claim 18, and thereby inherits all of the rejected limitations of claim 18.

34.2. Yamagishi appears to teach permitting one or more users to access the central database ***(page 13.2.1, figure 1)***.

Conclusion

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russell L. Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday - Friday 9:00 AM – 5:30 PM.

36. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 571-272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.

37. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RG

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